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(54) Title: Semiconductor Substrate, Field effect transistor, and their Manufacturing Methods

[*Insert graph. The vertical axis label = "Ge composition ratio, A". Horizontal axis label = "Thickness, B".*]

(57) Abstract: A semiconductor substrate comprises a Si substrate (1), a first SiGe layer (2) on the Si substrate, and a second SiGe layer (3) formed directly on the first SiGe layer (2) or with a Si layer being interposed therebetween. The thickness of the first SiGe layer is smaller than twice the critical thickness causing lattice relaxation due to dislocation caused when the film thickness is too large. The Ge composition ratio of the second SiGe layer is lower than the maximum value of the Ge composition ratio of the first SiGe layer at least at the contact surface in contact with the first SiGe layer or the Si layer. The second SiGe layer has at least a portion including a gradient composition region where the Ge composition ratio gradually increases toward the surface. As a result, the threading dislocation density and the surface roughness are reduced to practical levels.

(57) Abstract:
A semiconductor substrate comprises a Si substrate (1), a first SiGe layer (2) on the Si substrate, and a second SiGe layer (3) formed directly on the first SiGe layer (2) or with a Si layer being interposed therebetween. The thickness of the first SiGe layer is smaller than twice the critical thickness causing lattice relaxation due to dislocation caused when the film thickness is too large. The Ge composition ratio of the second SiGe layer is lower than the maximum value of the Ge composition ratio of the first SiGe layer at least at the contact surface in contact with the first SiGe layer or the Si layer. The second SiGe layer has at least a portion including a gradient composition region where the Ge composition ratio gradually increases toward the surface. As a result, penetrating dislocation density and the surface roughness are reduced to practical levels.

Specification

Semiconductor Substrate, Field effect transistor, and their Manufacturing Methods

Technical Field

The present invention relates to a semiconductor substrate, field effect transistor, and their manufacturing methods, wherein the semiconductor substrate and field effect transistor are used for high speed MOSFET and the like.

Background of the Technology

In recent years, high speed MOSFETs, MODFETs, and HEMTs have been proposed in which a strained Si layer, which has been grown epitaxially on a Si (silicon) wafer with a SiGe (silicon germanium) layer disposed therebetween, is used for the channel region. In this type of strained Si-FET, tensile strain occurs in the Si layer due to the SiGe which has a larger lattice constant in comparison to Si, and as a result, the Si band structure changes, degeneracy disappears, and carrier mobility increases. Therefore use of this strained Si layer for the channel region typically makes possible a 1.5- to 8-fold increase of speed. Furthermore, a typical Si substrate produced by the CZ method (Czochralski method) can be used as the substrate for the process, and a high speed CMOS device can be realized using conventional CMOS processes.

However, for epitaxial growth of the above mentioned strained Si layer for use as the desired FET channel region, a good quality SiGe layer must be grown by epitaxial growth on the Si substrate. Unfortunately, due to the difference between the lattice constants of Si and SiGe, crystallinity has been a problem due to dislocations and the like. Thus various types of below mentioned countermeasures have been proposed.

For example, these proposed methods include a method utilizing a buffer layer in which the Ge composition ratio of the SiGe is changed with a constant gentle gradient, a method utilizing a buffer layer in which the Ge (germanium) composition ratio is altered in a series of steps (step-wise), a method utilizing a buffer layer in which the Ge composition ratio is altered to a super lattice state, and a method utilizing a Si off-cut wafer and a buffer layer in which the Ge composition ratio is altered with a constant gentle gradient (U.S. Patent No. 5,442,205, U.S. Patent No. 5,221,413, PCT WO98/00857, Japanese Laid-open Unexamined Patent Application No. Hei 6-252046, etc.).

However, the following problems remain for the above mentioned conventional techniques.

That is to say, threading dislocation density and surface roughness of the SiGe layer grown using the above mentioned conventional techniques fail to attain the desired levels for a device and production process.

For example, when a buffer layer is used in which the Ge composition ratio varies at a gradient, although the penetrating dislocation density can be kept comparatively low, the surface roughness deteriorates. In contrast, when a buffer layer is used in which the Ge composition ratio varies in a step-wise manner, although the surface roughness is comparatively low, the resultant penetrating dislocation density becomes large. Moreover, when an off-cut wafer is used, dislocations tend to migrate laterally rather than in the direction of the film growth, but once again a sufficiently low degree of dislocation is unachievable. Surface roughness also does not reach the level required for photolithographic processing of modern LSI devices and the like.

Disclosure of the Invention

In consideration of the above mentioned problems, the object of the present invention is to provide a semiconductor substrate, a field effect transistor, and methods for production of the semiconductor substrate and field effect transistor that are capable of reducing penetrating dislocation density and surface roughness to levels sufficient for practical use.

In order to resolve the problems detailed above, the present invention adopts the configuration described below. That is to say, the semiconductor substrate of the present invention comprises a Si substrate, a first SiGe layer on the Si substrate, and a second SiGe layer disposed on the first SiGe layer or with an optional Si layer therebetween; wherein thickness of the first SiGe layer is smaller than twice the critical thickness causing lattice relaxation due to dislocations caused by increase of layer thickness; Ge composition ratio of the second SiGe layer is less than the maximum value of the Ge composition ratio of at least the first SiGe layer or the first SiGe layer at the interface with the Si layer; and at least a portion of the second SiGe layer has a gradient composition region such that the Ge composition ratio gradually increases toward the surface.

A method for production of a semiconductor substrate according to the present invention is a method of epitaxial growth of a SiGe layer on a silicon substrate comprising the steps of: performing a first layer forming step of epitaxial growth of a first SiGe layer on the Si substrate, and performing a second layer forming step of epitaxial growth of a second SiGe layer

directly on the first SiGe layer or with an optional epitaxial Si layer therebetween, wherein during the first layer forming step thickness of the first SiGe layer is set to be smaller than twice the critical thickness causing lattice relaxation due to dislocations caused by increase of layer thickness, and during the second layer forming step, the second SiGe layer is formed such that Ge composition ratio of the second SiGe layer is less than the maximum value of the Ge composition ratio of at least the first SiGe layer or the first SiGe layer at the interface with the Si layer, and at least a portion of the second SiGe layer has a gradient composition region such that the Ge composition ratio gradually increases toward the surface.

Moreover, the semiconductor substrate of the present invention is a semiconductor substrate having a SiGe layer formed on a Si substrate, wherein the semiconductor substrate is formed by the above mentioned production method of a semiconductor substrate of the present invention.

In order to resolve the problems detailed above, the present invention adopts the configuration described below. That is to say, the semiconductor substrate of the present invention is a semiconductor substrate comprising a Si substrate, a first SiGe layer on the Si substrate, and a second SiGe layer disposed on the first SiGe layer or with an optional Si layer therebetween, wherein thickness of the first SiGe layer is smaller than twice the critical thickness causing lattice relaxation due to dislocations caused by increase of layer thickness; the second layer SiGe layer has a multi-layered structure formed by alternately and contiguously stacking of a SiGe gradient layer having a Ge composition ratio that increases gradually toward the surface and thereupon a SiGe layer of constant composition having the same Ge composition ratio as the upper interface of the gradient composition layer, and the Ge composition ratio of the bottom interface of the second SiGe layer is less than the maximum value of the Ge composition ratio within the first SiGe layer.

The method for production of a semiconductor substrate according to the present invention is a method for production of a semiconductor substrate by epitaxial growth of a SiGe layer on a silicon substrate comprising the steps of: performing a first layer forming step of epitaxial growth of a first SiGe layer on the Si substrate, and performing a second layer forming step of epitaxial growth of a second SiGe layer directly on the first SiGe layer or with an optional epitaxial Si layer therebetween, wherein during the first layer forming step, thickness of the first SiGe layer is set to be smaller than twice the critical thickness causing lattice relaxation due to dislocations caused by increase of layer thickness, the second SiGe layer forming step, to form the second SiGe layer

such that Ge composition ratio has a gradient in the layer growth direction and changes step-wise, consists of repeating the following alternating steps a multiple number of times with a continuous Ge ratio: a step of epitaxial growth of a gradient composition layer of SiGe such that the Ge composition ratio increases gradually toward the surface, and a step of epitaxial growth of the constant composition layer of SiGe on the gradient composition layer at the final Ge composition ratio of the gradient composition layer, and Ge composition ratio of the bottom interface of the second SiGe layer is lower than the maximum value of the Ge composition ratio in the first SiGe layer.

Moreover, the semiconductor substrate of the present invention is a semiconductor substrate having a SiGe layer formed on a Si substrate, wherein the semiconductor substrate is formed by the above mentioned production method of a semiconductor substrate of the present invention.

This semiconductor substrate and production method for a semiconductor substrate set thickness of the first SiGe layer to be smaller than twice the critical thickness causing lattice relaxation due to dislocations caused by increase of layer thickness, lower Ge composition ratio of the second SiGe layer such that it is less than the maximum value of the Ge composition ratio of at least the first SiGe layer or of the first SiGe layer at the interface with the Si layer, and have at least a portion of the second SiGe layer that is a gradient composition region such that the Ge composition ratio gradually increases toward the surface. Moreover, since Ge composition ratio of the bottom interface of the second SiGe layer is made less than the maximum value of the Ge composition ratio in the first SiGe layer, it becomes possible for dislocations to be concentrated efficiently at the interface between the Si substrate and the first SiGe layer and at the interface between the first SiGe layer and the second SiGe layer, and it becomes possible to lower penetrating dislocation density and surface roughness of the second SiGe layer surface.

That is to say, due to growth of a layer for the first SiGe layer that is thinner than two times the critical thickness, dislocations mostly do not arise although strain energy increases in response to film thickness within the first SiGe layer. When epitaxial growth of the second SiGe layer begins thereafter, strain energy has already accumulated in the first SiGe layer, and thus during the stage when the second SiGe layer thickness is low, dislocations are generated and grow beginning at interfaces on both sides of first SiGe layer and within second SiGe layer on the first SiGe layer-side, and lattice relaxation begins in the first SiGe layer and in the second SiGe layer. During this time, due to lowering of Ge composition ratio of the second SiGe layer such that it is less than the maximum value of the Ge composition ratio of at least first SiGe layer or of the first SiGe layer at the interface with the Si layer, dislocations collect and grow along both interfaces of the first SiGe layer, growth of dislocations at both interfaces of the first SiGe layer helps lattice relaxation of the second SiGe layer, growth of dislocations in the second SiGe

layer is suppressed, and deterioration of surface roughness of the second SiGe layer is suppressed.

Furthermore, the first SiGe layer functions as a layer that removes impurities that occur at the Si substrate surface such as moisture, oxygen, and carbon. This has the effect of suppressing defects caused by surface contamination of the Si substrate.

Furthermore, in the gradient composition region of the second SiGe layer, dislocations are generated uniformly, dislocations become entangled, dislocation density decreases in the gradient composition region, and dislocation growth is induced in the lateral direction. This thus has the effect of decreasing the density of threading dislocations in the surface region and suppressing deterioration of surface roughness.

In the conventional case of a gradient composition region that lacks a first SiGe layer, dislocations begin to be generated when layer thickness of the gradient composition region exceeds the critical layer thickness and increases beyond a certain layer thickness. Once dislocation density has gone through an increase, the above mentioned effects are obtained as the gradient composition region is formed further. That is to say, the above mentioned effects are obtainable by the conventional structure only for the upper part of the gradient composition region.

However, according to the structure of the present invention that has a first SiGe layer, strain energy is previously accumulated in the first SiGe layer. Thus dislocation growth begins in the second SiGe layer at a stage when film thickness of the second SiGe layer is low and the above mentioned effects can be obtained over the entire gradient composition region of the second SiGe layer. Threading defect density in the surface region of the second SiGe layer is decreased, and deterioration of surface roughness is suppressed.

Furthermore, the first SiGe layer functions as a layer that removes impurities that occur at the Si substrate surface such as moisture, oxygen, and carbon. This has the effect of suppressing defects caused by surface contamination of the Si substrate.

Also when dislocations begin to be generated during the growth of the first SiGe layer, these dislocations begin to grow in various directions. Thus it becomes difficult to control the direction of dislocation growth, and reduction of penetrating defects and surface roughness is difficult. Thus it is necessary to set layer thickness of the first SiGe layer in a range that does not exceed twice the critical thickness and that is thinner than the layer thickness at which dislocation generation and lattice relaxation actually become conspicuous. At the same time, layer thickness of the first SiGe layer is effective when this thickness is in the vicinity of the layer thickness at which dislocation generation and lattice relaxation actually begin. The layer thickness for which dislocation generation and lattice relaxation actually begins differs according to layer growth temperature and other conditions. Thus for the respective layer growth conditions, layer thickness is preferably selected to obtain effectively the effects of the present invention by use of layer thickness in the vicinity of that at which dislocation generation and lattice relaxation begin to become conspicuous and within a range that does not exceed twice the critical layer thickness.

Moreover, due to use of the second layer SiGe layer that has a multi-layered structure formed by alternately stacking of a SiGe gradient layer having a Ge composition ratio that increases gradually toward the surface and thereupon a SiGe layer of constant composition having the same Ge composition ratio as the upper interface of the gradient composition layer, the entire

second SiGe layer becomes a layer having a Ge composition ratio of stepped gradient structure. Dislocations tend to propagate along the lateral direction, it becomes difficult for penetrating defects to be generated, and there is little change in composition at interfaces. Thus generation of dislocations at the interface is suppressed, dislocations are uniformly generated in the gradient composition layers, and it becomes possible to suppress deterioration of surface roughness.

As a result of research carried out by the inventors of the present invention concerning layer growth technology of SiGe, it was found that dislocations in crystals have the following tendencies.

That is to say, during layer formation of the SiGe layer, dislocations generated within the layer display a tendency to propagate either at an oblique angle relative to the direction of the layer formation, or in a lateral direction (in a direction orthogonal with the direction of the layer formation: direction <110>). Moreover, the dislocations tend to propagate in a lateral direction at a layer interface. However, at those interfaces where the composition alters suddenly, it is thought that the dislocations are more likely to propagate in the aforementioned oblique direction, and many dislocations will be generated in high density.

Therefore if layer formation is carried out using a simple step-wise Ge composition ratio, then it is thought that high densities of dislocations will tend to be generated at the interface parts where a sudden variation in composition occurs, that the dislocations will likely propagate at an oblique angle relative to the direction of layer formation, and these dislocations will become penetrating dislocations. Furthermore, if layer formation is carried out simply using a gently graded Ge composition ratio, then it is thought that the lack of areas (interfaces and the like) that offer an opportunity for the oblique dislocations to exit in a lateral direction means that the dislocations will penetrate through to the surface.

In contrast, the semiconductor substrate production method of the present invention repeats alternating steps of epitaxial growth of a SiGe gradient composition layer such that the Ge composition ratio increases gradually toward the surface and epitaxial growth of a SiGe constant composition layer on the gradient composition layer at the final Ge composition ratio of the gradient composition layer. Due to step-wise growth of the second SiGe layer that has a gradient of the Ge composition ratio in the layer growth direction, the resulting layer has a gradient stepped structure due to repeated step-wise alternating formation of gradient composition layers and constant composition layers. This is capable of forming a SiGe layer that has low dislocation density and low surface roughness.

That is to say, dislocations tend to propagate in the lateral direction, and it becomes difficult for penetrating dislocations to occur. Also due to the low change in composition ratio at an interface, generation of dislocations at the interface is suppressed, dislocations are generated uniformly within the gradient composition layer, and it becomes possible to suppress deterioration of surface roughness.

Furthermore, in the gradient composition region of the second SiGe layer, dislocations are generated uniformly, dislocations become entangled, dislocation density decreases in the gradient composition region, and dislocation growth is induced in the lateral direction. This thus has the effect of decreasing the density of penetrating dislocations in the surface region and suppressing deterioration of surface roughness.

In a conventional gradient composition region that lacks a first SiGe layer, dislocations begin to be generated when layer thickness of the gradient composition region exceeds the critical layer thickness and increases beyond a certain layer thickness. Once dislocation density has increased, the above mentioned effects are obtained if the gradient composition region is formed further. That is to say, the above mentioned effects are obtainable by the conventional structure only for the upper part of the gradient composition region.

However, according to the structure of the present invention that has a first SiGe layer, strain energy is previously accumulated in the first SiGe layer. Thus dislocation growth begins in the second SiGe layer at a stage when film thickness of the second SiGe layer is low, and the above mentioned effects can be obtained over the entire gradient composition region of the second SiGe layer. Penetrating defect density in the surface region of the second SiGe layer is decreased, and deterioration of surface roughness is suppressed.

Moreover, the semiconductor substrate of the present invention has adopted a technique wherein Ge composition ratio x of the first SiGe layer is constant, and thickness of the first SiGe layer is less than twice a critical layer thickness t_c that satisfies the following equations:

t_c (nm) = $(1.9 \times 10^{-3}/\varepsilon\,(x)^2) \cdot \ln(t_c/0.4)$,

$\varepsilon\,(x) = (a_0 + 0.200326x + 0.026174x^2)/a_0$), and

a_0 = 0.543 nm (a_0 is the Si lattice constant).

Furthermore, the method for production of a semiconductor substrate of the present invention adopts a technique wherein Ge composition ratio x of the first SiGe layer during the first formation step is constant, and thickness of the first SiGe layer is less than twice a critical layer thickness t_c that satisfies the following equations:

t_c (nm) = $(1.9 \times 10^{-3}/\varepsilon (x)^2) \cdot \ln(t_c/0.4)$,
$\varepsilon (x) = (a_0 + 0.200326x + 0.026174x^2)/a_0$), and
a_0 = 0.543 nm (a_0 is the Si lattice constant).

This semiconductor substrate and production method for a semiconductor substrate, due to the constant Ge composition ratio of the first SiGe layer, results in the thinnest layer thickness possible for the start of actual dislocation growth and lattice relaxation at that same Ge composition ratio, and the effect of the present invention can be obtained with the thinnest layer thickness possible. This has the advantage of shortening the time period required for layer growth. Moreover, according to this semiconductor substrate and production method for a semiconductor substrate, by setting the thickness of the first SiGe layer to less than twice the critical layer thickness t_c that satisfies the above mentioned equations (thickness that is taken to mean the layer thickness at which dislocations are generated and lattice relaxation occurs as calculated from the Ge composition ratio and lattice constant, regardless of the layer growth temperature), it becomes possible to readily set the first SiGe layer thickness within the thickness range at which generation of dislocations and lattice relaxation begin to actually become conspicuous.

That is to say, since the above mentioned layer thickness at which generation of dislocations and lattice relaxation begin to actually become conspicuous changes according to layer temperature, the thickness is set to less than twice the theoretical critical layer thickness t_c determined from just the Ge composition ratio x and lattice constant, this is less than the layer thickness at which actual generation of dislocations and lattice relaxation become conspicuous, and it becomes possible to obtain the effects of the present invention. Moreover, since the above mentioned critical layer thickness assumes layer growth under equilibrium conditions, just the Ge composition ratio and the lattice constant determine the critical layer thickness and the layer growth temperature is ignored. The layer thickness, however, at which actual dislocation generation and lattice relaxation become conspicuous also includes the case of growth in non-equilibrium states of low temperature growth and the like, not just equilibrium growth, and therefore is determined according to the layer temperature.

Moreover, the semiconductor substrate of the present invention preferably has a Ge composition ratio x of the first SiGe layer that is greater than or equal to 0.05 and less than or equal to 0.3.

Moreover, in the method for production of a semiconductor substrate of the present invention, the Ge composition ratio x of the first SiGe layer preferably is greater than or equal to 0.05 and less than or equal to 0.3.

Furthermore, in the method for production of a semiconductor substrate of the present invention, a strained Si layer is formed on a Si substrate with a SiGe layer therebetween, wherein the strained Si layer is formed preferably by epitaxial growth directly on the second SiGe layer, or with another SiGe layer therebetween.

The semiconductor substrate of the present invention is a semiconductor substrate having a SiGe layer formed on a Si substrate, and this semiconductor substrate of the present invention is produced by the above mentioned semiconductor substrate production method of the present invention. That is to say, since this semiconductor substrate is produced by the above mentioned semiconductor substrate production method of the present invention, there are few penetrating dislocations at the surface, and this semiconductor substrate has good surface roughness characteristics.

According to this semiconductor substrate and this semiconductor substrate production method, due to Ge composition ratio x of the first SiGe layer being greater than or equal to 0.05 and less than or equal to 0.3, layer thickness is neither excessively thick nor excessively thin for the start of actual dislocation generation and lattice relaxation, and the effects of the present invention are effectively obtained by a first SiGe layer of suitable thickness.

That is to say, if the Ge composition ratio x of the first SiGe layer is smaller than 0.05,the layer thickness at which actual dislocation generation and lattice relaxation start will be excessively thick, thereby increasing the time period required for layer growth of the first SiGe layer. Moreover, the resultant surface roughness of the first SiGe layer will deteriorate.

However, if the Ge composition ratio x of the first SiGe layer is larger than 0.3,the layer thickness at which actual dislocation generation and lattice relaxation start will be excessively thin, and it will be difficult to form the first SiGe layer with good controllability.

Moreover, if the Ge composition ratio x of the first SiGe layer is greater than or equal to 0.05 and is less than or equal to 0.3, thickness becomes suitable for the start of actual dislocation generation and lattice relaxation, dislocations will be generated mainly along both interfaces of the first SiGe layer, and growth of dislocations at both interfaces of the first SiGe layer effectively aids the lattice relaxation of the second SiGe layer.

Moreover, the semiconductor substrate of the present invention adopts a structure wherein the second SiGe layer is disposed directly on the first SiGe layer, and the entire second SiGe layer is a gradient composition layer having a Ge composition ratio that increases gradually in the direction of the surface.

Furthermore, the method for production of a semiconductor substrate of the present invention adopts a structure wherein the second SiGe layer is disposed directly on the first SiGe layer, and the entire second SiGe layer is a gradient composition layer having a Ge composition ratio that increases gradually in the direction of the surface.

Moreover, the semiconductor substrate of the present invention is a semiconductor substrate having a SiGe layer formed on a Si substrate, wherein the semiconductor substrate is produced by the above mentioned semiconductor substrate production method of the present invention.

The semiconductor substrate of the present invention has a strained Si layer formed by epitaxial growth directly on the second SiGe layer or with an optional SiGe layer therebetween.

The method for production of the semiconductor wafer of the present invention has a process for epitaxially growing a strained Si layer directly on the second SiGe layer or with an optional SiGe layer therebetween.

Moreover, the semiconductor wafer of the present invention is a semiconductor wafer having a strained Si layer formed on a Si substrate with a SiGe layer therebetween, and the semiconductor wafer is produced by the above mentioned method for production of the semiconductor wafer of the present invention.

According to this semiconductor substrate and this semiconductor substrate production method, the second SiGe layer is disposed directly on the first SiGe layer, and the entire second SiGe layer is a gradient composition layer for which the Ge composition ratio increases gradually toward the surface. This is advantageous in that the layers necessary for obtaining the effects of the present invention are not disposed wastefully, the effects of the present invention are obtained by the thinnest layers possible, and the time period required for layer growth is shortened.

According to this semiconductor substrate and this semiconductor substrate production method, the strained Si layer is formed by epitaxial growth directly on the second SiGe layer or with an optional SiGe layer therebetween. Thus a high quality strained Si layer is obtained that has few defects and low surface roughness, and it is possible to obtain a semiconductor substrate suitable for use with integrated circuits utilizing MOSFETs and the like that use a strained Si layer as the channel region.

The semiconductor substrate of the present invention has a strained Si layer formed by epitaxial growth directly on the above mentioned SiGe layer or with an optional additional SiGe layer therebetween.

Moreover, the method for production of the semiconductor wafer of the present invention epitaxially grows a strained Si layer directly on the above mentioned SiGe layer or with an optional additional SiGe layer therebetween.

Moreover, the semiconductor wafer of the present invention is a semiconductor wafer having a strained Si layer formed on a Si substrate with a SiGe layer therebetween, and the semiconductor substrate is produced by the above mentioned method for production of the semiconductor wafer that grows the strained Si layer of the present invention.

According to this semiconductor substrate and this semiconductor substrate production method, the strained Si layer is formed by epitaxial growth directly on the SiGe layer or with an optional other SiGe layer therebetween. Thus a high quality

strained Si layer is obtained that has few defects and low surface roughness, and it is possible to obtain a semiconductor substrate suitable for use with integrated circuits utilizing MOSFETs and the like that use a strained Si layer as the channel region.

The field effect transistor of the present invention is a field effect transistor having a channel region in a strained Si layer on a SiGe layer, wherein the field effect transistor has the channel region in the strained Si layer of the above mentioned semiconductor substrate of the present invention.

Moreover, the method for production of a field effect transistor of the present invention is a method for production of a field effect transistor having a channel region in a strained Si layer formed by epitaxial growth on a SiGe layer, wherein the channel region is formed in the strained Si of the semiconductor substrate produced according to the above mentioned semiconductor substrate production method of the present invention.

Moreover, the field effect transistor of the present invention is a field effect transistor having a channel region formed in a strained Si layer formed by epitaxial growth on a SiGe layer, wherein the field effect transistor is produced by the above mentioned field effect transistor production method of the present invention.

The production method for the field effect transistor of the present invention is a method for production of a field effect transistor that has a channel region in a strained Si layer formed by epitaxial growth on a SiGe layer, wherein the channel region is formed in the strained Si of the semiconductor substrate produced according to the above mentioned method for production of a semiconductor substrate having the strained Si layer of the present invention.

Moreover, the field effect transistor of the present invention is a field effect transistor having a channel region formed in a strained Si layer formed by epitaxial growth on a SiGe layer, wherein the field effect transistor is produced by the above mentioned production method for the field effect transistor of the present invention.

According to this field effect transistor and this field effect transistor production method, the channel layer is formed in the above mentioned strained Si layer of the semiconductor substrate of the present invention or the semiconductor substrate produced according to the above mentioned semiconductor substrate production method of the present invention. Thus it is possible to obtain field effect transistors that have good characteristics at high yield due to the good quality of the strained Si layer.

Simple Explanation of the Figures

Figure 1 is a cross-sectional diagram showing a semiconductor substrate of the working example no. 1 of the present invention.
Figure 2 is a graph showing Ge composition ratio plotted against semiconductor substrate layer thickness of the working example no. 1 of the present invention.
Figure 3 is a cross-sectional schematic diagram showing a MOSFET of the working example no. 1 of the present invention.
Figure 4 is a graph showing Ge composition ratio plotted against semiconductor substrate layer thickness of the working example no. 2 of the present invention.
Figure 5 is a graph showing Ge composition ratio plotted against semiconductor substrate layer thickness of the working example no. 3 of the present invention.
Figure 6 is a graph showing Ge composition ratio plotted against semiconductor substrate layer thickness of the working example no. 4 of the present invention.
Figure 7 is a graph showing Ge composition ratio plotted against semiconductor substrate layer thickness of the working example no. 5 of the present invention.
Figure 8 is a graph showing results of SIMS-based analysis of the distribution of Ge composition ratio versus layer thickness for a substrate having 300 nm layer thickness for the first SiGe layer of a semiconductor substrate that is a working example corresponding to working example no. 1 of the present invention.
Figure 9 is a graph showing penetrating dislocation density versus layer thickness of the first SiGe layer of a working example corresponding to working example no. 1 of the present invention.
Figure 10 is a graph showing surface roughness versus layer thickness of the first SiGe layer of a working example corresponding to working example no. 1 of the present invention.
Figure 11 is a microscopic photograph of the surface of a conventional example according to the present invention. [*TRANSLATOR'S NOTE: This caption seems to be an error in the source text. How could there be a conventional example of the present invention?*]
Figure 12 is a microscopic photograph of the surface of a working example corresponding to working example 1 of the present invention.
Figure 13 is a table showing respective surface roughness values for working examples corresponding to working example no. 2 through 5 of the present invention.
Figure 14 is a graph showing measurement results for penetrating dislocation density versus layer thickness of the first SiGe layer for a working example corresponding to working example no. 2 of the present invention.
Figure 15 is a graph showing measurement results for surface roughness versus layer thickness of

the first SiGe layer for a working example corresponding to working example no. 2 of the present invention.
Figure 16 is a graph showing Ge composition ratio versus layer thickness of a semiconductor substrate for working example no. 1 according to the present invention.
Figure 17 is a cross-sectional diagram showing the second SiGe layer for working example no. 1 according to the present invention.
Figure 18 is a graph showing Ge composition ratio versus layer thickness of the second SiGe layer for working example no. 1 according to the present invention.
Figure 19 is a graph showing Ge composition ratio versus layer thickness of the second SiGe layer for working example no. 2 according to the present invention.
Figure 20 is a cross-sectional diagram showing the second SiGe layer for working example no. 2 according to the present invention.
Figures 21A through 21D are graphs showing the Ge composition ratio versus layer thickness of the first SiGe layer for various embodiments of working example no. 3 according to the present invention.
Figure 22 is a graph showing measurement results for penetrating dislocation density when layer thickness is changed relative to the first SiGe layer for working example no. 1 according to the present invention.
Figure 23 is a graph showing results of surface roughness measurement when layer thickness is changed relative to the first SiGe layer for working example no. 1 according to the present invention.
Figures 24A through 24G are TEM (transmission electron microscope) images that show observed results of the layer growth process.

Best Mode for Carrying Out the Present Invention

Working example no. 1 according to the present invention is explained below while referring to Figure 1 through Figure 3.

Figure 1 shows the cross-sectional structure of a semiconductor wafer (semiconductor substrate) W of the present invention. This structure of the semiconductor wafer will be explained together with the production process thereof. First, on a p-type or n-type Si substrate 1 that has been fabricated by a pull-up growth method such as the CZ method, as shown in Figure 1 and Figure 2, a first SiGe layer 2 having a constant Ge composition ratio x (e.g. $x = 0.15$) is grown epitaxially using, for example, low pressure CVD to form a layer (e.g. 300 nm) that is thinner than the layer thickness at which above mentioned actual dislocation generation and lattice relaxation begin to be conspicuous.

At this time, since first SiGe layer 2 is grown to a layer thickness thinner than the layer

thickness at which actual dislocation generation and lattice relaxation begin to be conspicuous, although strain energy increases with increased layer thickness during growth of the first SiGe layer 2, dislocations and lattice relaxation are nearly absent.

Furthermore, thickness of first SiGe layer 2 is less than twice the critical layer thickness t_c that satisfies the following equations:

t_c (nm) = $(1.9 \times 10^{-3}/\varepsilon (x)^2) \cdot \ln(t_c/0.4)$,

$\varepsilon (x) = (a_0 + 0.200326x + 0.026174x^2)/a_0$), and

a_0 = 0.543 nm (a_0 is the Si lattice constant).

Next a second SiGe layer 3 is formed by epitaxial growth on first SiGe layer 2. Ge composition ratio y of this second SiGe layer 3, at least at the interface with the first SiGe layer 2, is set to a value lower than the maximum value of Ge composition ratio x occurring in first SiGe layer 2. Moreover, second SiGe layer 3 is a gradient composition layer (gradient composition region) in which the Ge composition ratio y gradually increases in the direction of the surface (e.g., Ge composition ratio y increases from 0 to 0.3 in the layer). This layer is formed to a thickness, for example, of 1.1 μm.

When epitaxial growth of second SiGe layer 3 is started, due to previous accumulation of strain energy in first SiGe layer 2, dislocations are generated and grow at a stage when layer thickness of second SiGe layer 3 is thin. These dislocations are generated and grow beginning at both interfaces of first SiGe layer 2 and in the first SiGe layer 2 side of second SiGe layer 3, and lattice relaxation starts at first SiGe layer 2 and second SiGe layer 3. At this time, the Ge composition ratio of second SiGe layer 3 at the interface with first SiGe layer 2 has a value lower than the maximum value of the Ge composition ratio occurring in first SiGe layer 2. Therefore although dislocations are generated and concentrate along interfaces 2a and 2b at both sides of first SiGe layer 2, lattice relaxation of second SiGe layer 3 is aided, generation and growth of dislocations in second SiGe layer 3 is suppressed, and deterioration of surface roughness of second SiGe layer 3 is suppressed.

In addition, a SiGe relaxation layer 4 is formed by epitaxial growth to a certain thickness (e.g., 0.75 μm) at a constant Ge composition ratio z (e.g. z = 0.3) that is the same as the final Ge composition ratio of second SiGe layer 3. Thereafter single crystal Si is formed by epitaxial growth on this SiGe relaxation layer 4 as a strained layer 5 of just a certain thickness (e.g.,

20 nm), thus producing a semiconductor wafer W of the present working example.

Furthermore, layer growth by the above mentioned low pressure CVD utilizes H_2 as the carrier gas and utilizes SiH_4 and GeH_4 as source gases.

In semiconductor wafer W of the present working example produced in this manner, first SiGe layer 2 has a film thickness that is set to be thinner than that at which actual dislocation generation and lattice relaxation begin to become conspicuous, and the Ge composition ratio y of second SiGe layer 3, at least at the interface with the first SiGe layer 2, is lower than the intra-layer maximum value of Ge composition ratio x in first SiGe layer 2. Therefore dislocations can be efficiently concentrated at interface 2a between Si substrate 1 and first SiGe layer 2 and at interface 2b between first SiGe layer 2 and second SiGe layer 3, and it is possible to decrease penetrating dislocation density and surface roughness.

Moreover, first SiGe layer 2 has a constant Ge composition ratio and this is advantageous in that the layer thickness at which actual dislocation generation and lattice relaxation begin to become conspicuous becomes as thin as possible, the effects of the present invention are obtained at the thinnest layer thickness possible, and the time required for layer growth is short.

Moreover, by setting first SiGe layer 2 to a thickness less than twice the critical layer thickness t_c that satisfies the above mentioned relationships, based upon the below mentioned experimental results, it is possible to set first SiGe layer 2 readily to a layer thickness within the layer thickness at which actual dislocation generation and lattice relaxation begin to be conspicuous.

Moreover, according to the present working example, second SiGe layer 3 is a gradient composition layer (gradient composition region) for which the Ge composition ratio gradually increases. Thus dislocations are generated uniformly, entanglement between dislocations occurs, and dislocation density in second SiGe layer 3 decreases. Also dislocations are induced to grow laterally. This has the effect of decreasing the density of penetrating dislocations in the surface region and suppressing deterioration of surface roughness.

Moreover, since strain energy accumulated previously in the first SiGe layer 2 prior to growth of second SiGe layer 3 in the present working example, dislocation generation in second SiGe layer 3 begins at a stage when layer thickness of second SiGe layer 3 is thin, and the above mentioned effects are obtained for the entire gradient composition region in second SiGe layer 3. Penetrating dislocation density in the surface region of second SiGe layer 3 decreases, and deterioration of second SiGe layer 3 surface roughness is suppressed.

Furthermore, the first SiGe layer 2 functions as a layer that removes impurities at the Si substrate 1 surface such as moisture, oxygen, and carbon, and this has the effect of

suppressing defects causes by surface contamination of Si substrate 1.

A field effect transistor (MOSFET) of the present invention utilizing the above mentioned semiconductor wafer W and the production process of this field effect transistor will be explained together while referring to Figure 3.

Figure 3 schematically shows the structure of a field effect transistor of the present invention. During production of this field effect transistor, a SiO_2 gate oxide layer 6 and a gate polysilicon layer 7 are stacked in order on the strained Si layer 5 of the surface of semiconductor wafer W produced by the above mentioned production process. Then a gate electrode (not shown in the figure) is formed by patterning on the gate polysilicon layer 7 above the part that becomes the channel region.

Thereafter the gate oxide layer 6 is also patterned, and areas outside those beneath the gate electrode are removed. Next, using the gate electrode as a mask, ion injection is performed and an n-type or p-type source region S and a drain region D are formed in a self-aligning manner on the strained Si layer 5 and the relaxation layer 4. Thereafter a source electrode and a drain electrode (not shown in the figure) are formed on the source region S and the drain region D respectively, thereby completing the production of an n-type or a p-type MOSFET in which the strained Si layer 5 becomes the channel region.

In a MOSFET produced in this manner, because the channel region is formed on the strained Si layer 5 of the semiconductor wafer W prepared by the production process described above, the superior quality of the strained Si layer 5 enables a high quality MOSFET to be produced with good yield.

Working example no. 2 according to the present invention will be explained next while referring to Figure 4.

The point of difference between the working example no. 1 and working example no. 2 is that whereas first SiGe layer 2 of working example no. 1 has its Ge composition ratio set to a constant value, as shown in Figure 4, the Ge composition ratio x of first SiGe layer 12 of working example no. 2 has a gradually decreasing Ge composition ratio x having its intra-layer maximum value at the interface with Si substrate 1.

That is to say, during the first SiGe layer 12 formation step of the present working example, the Ge composition ratio x at the beginning of layer growth is set to 0.2, and thereafter Ge composition ratio x decreases gradually until reaching nearly zero. A gradient composition layer is grown of just a certain thickness (e.g., 350 nm) that is thinner than the layer thickness at which actual dislocation generation and lattice relaxation begin to become conspicuous.

For the present working example, the Ge composition ratio x of the first SiGe layer 12 is set to a maximum value in the layer at the interface with Si substrate 1. Thus strain energy during layer

growth becomes concentrated at the interface with Si substrate 1, and during lattice relaxation occurring at the start of layer growth of the second SiGe layer 3, more dislocations can be formed at the interface with Si substrate 1 than at the interface with second SiGe layer 3. By this means it becomes possible to concentrate dislocations at a position that is displaced from the surface side of second SiGe layer 3, and it also becomes possible to reduce penetrating dislocations and surface roughness in the same manner as during working example no. 1.

Working example no. 3 according to the present invention will be explained next while referring to Figure 5.

The point of difference between the working example no. 3 and working example no. 2 is that whereas first SiGe layer 2 of working example no. 2 is a gradient composition layer that has a gradually decreasing Ge composition ratio, as shown in Figure 5, the Ge composition ratio x of first SiGe layer 22 of working example no. 3 has a value of 0.2 at the beginning of layer formation, thereafter Ge composition ratio x gradually decreases during layer formation to nearly zero over a certain thickness (e.g. 175 nm), and thereafter the Ge composition ratio x gradually increases again to reach a final value of 0.2 during layer growth of a certain thickness (e.g., 175 nm).

Furthermore, thickness of this first SiGe layer 22 is also set thinner than the layer thickness at which actual dislocation generation and lattice relaxation begin to become conspicuous.

Also for this working example no. 3, the Ge composition ratio x of first SiGe layer 22 reaches its maximum value at the interfaces between Si substrate 1 and between second SiGe layer 3. Thus it becomes possible to generate many dislocations at the interface with Si substrate 1 and at the interface with second SiGe layer 3 in the same manner as in working example no. 1.

Working example no. 4 and working example no. 5 according to the present invention will be explained next while referring to Figure 6 and Figure 7.

The point of difference between the working example no. 4 and working example no. 1 is that whereas the Ge composition ratio of first SiGe layer 2 of working example no. 1 is constant, as shown in Figure 6, the Ge composition ratio x of first SiGe layer 32 of working example no. 4 increases gradually from a value of nearly zero to reach a final value of 0.2 at a certain layer thickness (e.g., 350 nm) that is thinner than the layer thickness at which actual dislocation generation and lattice relaxation begin to become conspicuous.

Moreover, the point of difference between the working example no. 5 and working example no. 1 is that whereas the Ge composition ratio of first SiGe layer 2 of working example no. 1 is constant, as shown in Figure 7, the Ge composition ratio x of first SiGe layer 42 of working example

no. 5 increases gradually from a value of nearly zero to a value of 0.2 over a certain thickness (e.g., 175 nm) of layer growth, and thereafter the Ge composition ratio x decreases gradually from 0.2 to nearly zero over a certain thickness (e.g., 175 nm) of layer formation. Furthermore, thickness of first SiGe layer 42 is set thinner than the layer thickness at which actual dislocation generation and lattice relaxation begin to become conspicuous.

Due to formation of both first SiGe layer 32 and 42 of this working example no. 4 and working example no. 5 respectively at a layer thickness that is thinner than the layer thickness at which actual dislocation generation and lattice relaxation begin to become conspicuous, dislocations are generated mainly at both interfaces of first SiGe layers 32 and 42 during layer formation of second SiGe layer 3, and it becomes possible to decrease penetrating dislocations and surface roughness. Furthermore, since the maximum intra-layer value of Ge composition ratio in the first SiGe layer 32 or 42 is not at the interface with Si substrate 1, working example no. 1 and working example no. 2 are better able to obtain improvement effects for penetrating dislocations and surface roughness.

Furthermore, the technological scope of the present invention is not limited to the embodiments of the above mentioned working examples. Various types of alterations can be added as long as these do not depart from the gist of the scope of the present invention.

For example, in the above working examples, a total of 5 types of distributions where used for the Ge composition ratio versus layer thickness in the first SiGe layer, but other distributions are also permissible. For example, it is also permissible for the first SiGe layer to have a multi-layer structure comprising multiple SiGe layers having differing Ge composition ratios. Moreover, it is possible for these multi-layer structures to include a Si layer.

Moreover, in all of the above mentioned working examples, although composition varied at a constant rate relative to layer thickness when Ge composition ratio was changed in the first SiGe layer, it is also permissible for this rate to be non-constant.

Furthermore, although the first SiGe layer is a layer that includes Ge and preferably accumulates strain energy, other distributions of the Ge composition ratio are also permissible.

Moreover, although during all of the above mentioned working examples, the entire second SiGe layer was a gradient composition layer for which the Ge composition ratio increased gradually, this layer may also be formed from gradient composition layers and uniform composition layers to produce a multi-layer structure. Moreover, the multiple layers may include a Si layer.

Moreover, in all of the above mentioned working examples, the Ge composition ratio within the second SiGe layer increased gradually toward the surface in a gradient composition region, and composition changed at a constant rate with respect to layer thickness. However, this rate may also be non-constant. Moreover, this composition gradient of the Ge composition ratio may also vary in a step-wise manner.

Moreover, although the second SiGe layer was disposed directly on the first SiGe layer in all of the above mentioned working examples, it is also possible for the second SiGe layer to be disposed on an intervening Si layer.

Moreover, it is possible for an additional SiGe layer to be formed on the strained Si layer of semiconductor wafer W of each of the above mentioned working examples.

Moreover, in all of the above mentioned working examples, a semiconductor wafer having a SiGe layer was produced as a substrate for MOSFET use. However, the wafer may also be used as a substrate that is suitable for use with other applications. For example, the semiconductor substrate and the semiconductor substrate production method of the present invention can be used appropriately for solar cell applications. That is to say, a solar cell substrate may be produced by forming a SiGe layer that is a gradient composition layer that has a gradually increasing Ge composition ratio so as to reach 100% Ge at the top-most surface of the Si substrate of each of the above mentioned working examples, followed by forming a GaAs (gallium arsenide) layer thereupon. In so doing, a high quality solar cell substrate with a low dislocation density is able to be prepared.

Moreover, according to the production method for a semiconductor substrate according to the present invention, it becomes possible to obtain a semiconductor substrate having a high quality SOI (silicon on insulator) structure that has few dislocations in the strained silicon. A semiconductor substrate having an SOI structure having strained silicon can be produced by the so-called "smart-cut" method. The smart-cut method is also called the "hydrogen implantation-delamination method". In this method, single silicon crystals are implanted using hydrogen ions, particularly positive ions, and a thin layer is cut away using the phenomenon of partial slicing of the silicon crystal lattice. A semiconductor substrate of the present application having a SOI structure (i.e. SiGe / SiO_2 / Si) produced in this manner can be used with advantage for the production of a SOI substrate as mentioned, for example, in US 5,906,951.

SIMS (secondary ion mass spectrometry) analysis results, penetrating dislocation density, surface roughness, and surface optical microscope image observation results will be explained next for semiconductor substrates actually produced according to the present invention.

Multiple semiconductor substrates corresponding to the above mentioned working example no. 1 were produced wherein the Ge composition ratio of the first SiGe layer was set to 0.1, 0.15, or 0.2 while layer thickness was varied. Furthermore, substrates were also produced by conventional technology (i.e., without the first SiGe layer) for the purpose of comparison.

Among these semiconductor substrates, Figure 8 shows results of SIMS analysis of the distribution of the Ge composition ratio with respect to layer thickness for a substrate having a first

SiGe layer thickness of 300 nm.

Respective measured results for penetrating dislocation density and surface roughness of these semiconductor wafers are shown in Figure 9 and Figure 10. Furthermore, penetrating dislocation density is indicated by etch pit density, and surface roughness is indicated by the RMS (root mean square) roughness.

As may be understood from these figures, in comparison to the case of the conventional technology (first SiGe layer of zero thickness), penetrating dislocation density and surface roughness were both low when layer thickness of the first SiGe layer was less than twice the critical layer thickness t_c.

Moreover, respective optical microscope images of the surfaces in the case of the conventional technology (first SiGe layer thickness of zero), and the case of a 180 nm-thick first SiGe layer that had a first SiGe layer Ge composition ratio of 0.2 among the above mentioned working examples, are shown in Figure 11 and Figure 12.

As may be understood from these figures, the present working example had much less etch pit dark spots than the conventional technology.

Furthermore, Figures 24A through 24G are TEM (transmission electron microscope) images that are the results of observation of the layer growth process. The progress of layer formation according to the conventional production method is shown in Figures 24A through 24C, and the progress of layer formation according to the method for production of a semiconductor substrate of the present patent application is shown in Figures 24D through 24G. Figure 24B and Figure 24E are images taken at the same point in time, and Figure 24C and Figure 24F are images taken simultaneously at a later time. Relaxation has not started for Figure 24C. In contrast, Figure 24F shows the generation of many dislocations at the interface between the first SiGe layer and the Si substrate and at the interface between the first SiGe layer and the second SiGe layer, while it can be recognized that there were extremely few dislocations at the surface side of the second SiGe layer, and relaxation was progressing at both interfaces of the first SiGe layer.

Moreover, semiconductor substrates were actually produced corresponding to the above mentioned working examples no. 2 through no. 5, surface roughness was measured in the same manner as above, and the results are shown in the table of Figure 13. Furthermore, the maximum Ge composition ratio of the first SiGe layer in each case was 0.2, and layer thickness was set to 350 nm. As may be understood from Figure 13, the working examples corresponding to working example no. 2 and working example no. 3 gave results that were superior to the other working examples. Respective results for penetrating dislocation density versus layer thickness of the first SiGe layer and surface roughness for the working example corresponding to working example no. 2 are shown in Figure 14 and Figure 15. In the same

manner as in the case of working example no. 1, in comparison to the case of the conventional technology (first SiGe layer thickness equal to zero), penetrating dislocation density and surface roughness were both reduced when layer thickness of the first SiGe layer was less than twice the critical layer thickness t_c.

Working example no. 6 according to the present invention is explained below while referring to Figures 1, 3, 16, 17, and 18.

Figure 1 shows the cross-sectional structure of the semiconductor wafer (semiconductor substrate) W of the present invention. The structure of this semiconductor wafer will be explained together with the production method thereof. First, on a p-type or n-type Si substrate 1 that has been fabricated by a pull-up growth method such as the CZ method, as shown in Figure 1 and Figure 16, a first SiGe layer 2 having a constant Ge composition ratio x (e.g. $x = 0.15$) is grown by epitaxy using, for example, low pressure CVD to form a thin layer (e.g. 300nm) that is thinner than the layer thickness at which above mentioned actual dislocation generation and lattice relaxation begin to be conspicuous.

At this time, since first SiGe layer 2 is grown to a layer thickness thinner than the layer thickness at which actual dislocation generation and lattice relaxation begin to be conspicuous, although strain energy increases with increased layer thickness during growth of the first SiGe layer 2, dislocations and lattice relaxation are nearly absent.

Furthermore, thickness of first SiGe layer 2 is less than twice the critical layer thickness t_c that satisfies the following equations:

$t_c\,(\mathrm{nm}) = (1.9 \times 10^{-3}/\varepsilon\,(x)^2) \cdot \ln(t_c/0.4)$,

$\varepsilon\,(x) = (a_0 + 0.200326x + 0.026174x^2)/a_0)$, and

$a_0 = 0.543$ nm (a_0 is the Si lattice constant).

Next a second SiGe layer 3 is formed by epitaxial growth on first SiGe layer 2. Ge composition ratio y of this second SiGe layer 3, at least at the interface with the first SiGe layer 2, is set to a value lower than the maximum value of Ge composition ratio x occurring in first SiGe layer 2. Moreover, second SiGe layer 3 is a stepped composition layer in which the Ge composition ratio x increases step-wise in the layer growth direction from 0 to y (e.g., $y = 0.3$) as stepped gradient layers of $Si_{1-x}Ge_x$.

Thereafter a $Si_{1-y}Ge_y$ relaxation layer 4 of constant Ge composition ratio is formed by

epitaxial growth on second SiGe layer 3. Furthermore, epitaxial growth is used to deposit Si on the $Si_{1-z}Ge_z$ relaxation layer 4 having a Ge composition ratio of z (for the present working example, z = y) to form a strained Si layer 5. Thus a semiconductor wafer W of the present invention is provided with a strained Si layer and fabricated. Furthermore, the various layer thicknesses, for example, are 1.5 μm for second SiGe layer 3, 0.7 - 0.8 μm for relaxation layer 4, and 15 - 22 nm for strained Si layer 5.

Formation of the above mentioned second SiGe layer 3, as shown in Figure 16 through Figure 18, is carried out by repeating the following processes a multiple number of times using continuous Ge composition ratios: performing epitaxial growth of a SiGe gradient composition layer 3a for which the Ge composition ratio increases gradually in the surface direction up to a certain value, and performing epitaxial growth on gradient composition layer 3a of a constant SiGe composition layer 3b at the final Ge composition ratio of gradient composition layer 3a. Moreover, the Ge composition ratio of the bottom surface of second SiGe layer 3 it set less than or equal to the Ge composition ratio of the upper surface of first SiGe layer 2. Furthermore, according to the present working example, the Ge composition ratio of second SiGe layer 3 increases gradually from zero.

For example, in the present working example, the epitaxial growth process of forming gradient composition layer 3a and constant composition layer 3b are repeated 5 times to form a second SiGe layer 3. That is to say, if a single gradient composition layer 3a and constant composition layer 3b epitaxial growth process is taken as 1 step, then during the initial step, a first gradient composition layer 3a is formed on Si substrate 1 so that the Ge composition ratio increases gradually from 0 to 0.06, then a first constant composition layer 3b is formed thereupon at a Ge composition ratio of 0.06. Thereafter during the second step, a second gradient composition layer 3a is formed on the first constant composition layer that has a Ge composition ratio of 0.06 so that Ge composition ratio gradually increases from 0.06 to 0.12 and then a second constant composition layer 3b is formed thereupon having a Ge composition ratio of 0.12.

Thereafter during the third step, a third gradient composition layer 3a is formed on the second constant composition layer 3b that has a Ge composition ratio of 0.12, and this layer is grown so that Ge composition ratio increases gradually from 0.12 to 0.18. A third constant composition layer 3b is formed thereupon having a Ge composition ratio of 0.18. Thereafter during the fourth step, a fourth gradient composition layer 3a is formed on the third constant composition layer 3b that has a Ge composition ratio of 0.18, and this layer is grown so that Ge composition ratio increases gradually from 0.18 to 0.24. A fourth constant composition layer 3b is formed thereupon having a Ge composition ratio of 0.24. Then during the final step, a fifth gradient composition layer 3a is formed on the fourth constant composition layer 3b that has a Ge composition ratio of 0.24, and this layer is grown so that Ge composition ratio increases gradually from 0.24 to 0.3. A fifth constant

become conspicuous becomes as thin as possible, the effects of the present invention are obtained at the thinnest layer thickness possible, and the time required for layer growth is short.

Moreover, by setting thickness of first SiGe layer 2 to less than twice the critical layer thickness t_c that satisfies the above mentioned relationships, based upon the below mentioned experimental results, it is possible to set first SiGe layer 2 readily to a layer thickness within the thickness range at which actual dislocation generation and lattice relaxation begin to be conspicuous in the layer.

Moreover, since strain energy accumulated previously in the first SiGe layer 2 prior to growth of second SiGe layer 3 in the present working example, dislocation generation in second SiGe layer 3 begins at a stage when layer thickness of second SiGe layer 3 is thin, and the above mentioned effects are obtained for the entire gradient composition region in second SiGe layer 3. Threading dislocation density in the surface region of second SiGe layer 3 decreases, and deterioration of second SiGe layer 3 surface roughness is suppressed.

Furthermore, first SiGe 2 layer functions as a layer that removes impurities that occur at the Si substrate 1 surface such as moisture, oxygen, and carbon. This has the effect of suppressing defects caused by surface contamination of the Si substrate.

Moreover, formation of second SiGe layer 3 in the present working example is carried out by repeating the following processes a multiple number of times at non-discontinuous Ge composition ratio: forming by epitaxial growth a SiGe gradient composition layer 3a that has a gradually increasing Ge composition ratio in the direction of the surface, and forming by epitaxial growth a SiGe constant composition layer 3b at a Ge composition ratio continuous with that of the previous process. Thus this layer is a stepped gradient layer formed by alternating gradient composition layer 3a and constant composition layer 3b. A SiGe layer can be formed in this manner that has a low dislocation density and low surface roughness.

That is to say, according to the present working example, the dislocations necessary for lattice relaxation are generated uniformly, and it is possible to grow a SiGe layer such that dislocations run along the lateral direction as much as possible without penetrating to the surface. Thus a good surface condition can be obtained.

A field effect transistor (MOSFET) of the present invention utilizing the above mentioned semiconductor wafer W and the production process of this field effect transistor will be explained together while referring to Figure 3.

Figure 3 schematically shows the cross-sectional structure of a field effect transistor of the present invention. During production of this field effect transistor, a SiO_2 gate oxide layer 6 and a gate polysilicon layer 7 are stacked in order on the strained Si layer 5 at the surface of

semiconductor wafer W produced by the above mentioned production process. Then a gate electrode (not shown in the figure) is formed by patterning on the gate polysilicon layer 7 above the part that becomes the channel region.

Thereafter the gate oxide layer 6 is also patterned, and areas outside those beneath the gate electrode are removed. Next, using the gate electrode as a mask, ion injection is performed and an n-type or p-type source region S and a drain region D are formed in a self-aligning manner on the strained Si layer 5 and the relaxation layer 4. Thereafter a source electrode and a drain electrode (not shown in the figure) are formed on the source region S and the drain region D respectively, thereby completing the production of an n-type or a p-type MOSFET in which the strained Si layer 5 becomes the channel region.

In a MOSFET produced in this manner, because the channel region is formed on the strained Si layer 5 on the semiconductor wafer W prepared by the production process described above, the good quality of the strained Si layer 5 enables a high quality MOSFET to be produced with high yield.

Working example no. 7 according to the present invention will be explained next while referring to Figure 19 and Figure 20.

Working example no. 7 differs from working example no. 6 in that, although layer thicknesses of each of the respective gradient composition layers 3a and constant composition layers 3b are the same for second SiGe layer 3 in working example no. 6, as shown in Figure 19 and Figure 20, during each repetition of the epitaxial growth steps of the gradient composition layer 13a and constant composition layer 13b of working example no. 7, thickness of each respective repeated gradient composition layer 13a and constant composition layer 13b gradually becomes thinner to form second SiGe layer 13. Furthermore, although the gradient composition layer 3a and constant composition layer 3b epitaxial growth steps in working example no. 1 are carried out repeatedly 5 times, in the present working example, the gradient composition layer 13a and constant composition layer 13b epitaxial growth steps are carried out repeatedly 4 times to form second SiGe layer 13.

That is to say, during the gradient composition layer 13a and constant composition layer 13b epitaxial growth steps of the present working example, a first gradient composition layer 13a and constant composition layer 13b are grown. Then a second gradient composition layer 13a and constant composition layer 13b are grown more thinly than the first gradient composition layer 13a and constant composition layer 13b. Then in the same manner, a third gradient composition layer 13a and constant composition layer 13b are grown more thinly than the second gradient composition layer 13a

and constant composition layer 13b. Then finally a fourth gradient composition layer 13a and constant composition layer 13b are grown more thinly than the third gradient composition layer 13a and constant composition layer 13b, thereby forming second SiGe layer 13.

That is to say, if the thicknesses of first gradient composition layer 13a and constant composition layer 13b are taken to be L_1, thicknesses of second gradient composition layer 13a and constant composition layer 13b are taken to be L_2, thicknesses of third gradient composition layer 13a and constant composition layer 13b are taken to be L_3, and thicknesses of fourth gradient composition layer 13a and constant composition layer 13b are taken to be L_4. Then these layers are stacked such that $L_1 \geq L_2 \geq L_3 \geq L_4$.

Furthermore, although the critical layer thickness for generation of dislocations varies according to the Ge composition ratio, each of the above mentioned layers is set to be thicker than this critical layer thickness so that dislocations necessary for lattice relaxation occur in each layer uniformly.

Moreover, the gradient of Ge composition ratio in each of the gradient composition layers 13a is set to the same value.

As explained previously, dislocations tend to be more readily generated as Ge composition ratio increases. Thus in the case of repeated layers of the same thickness as per working example no. 6, more of the resultant dislocations are generated in the uppermost layers. However, in this working example, due to gradual thinning of gradient composition layer 13a and constant composition layer 13b during each repetition, it becomes possible to generate dislocations uniformly in each layer.

Working example no. 8 according to the present invention will be explained next while referring to Figures 21A through 21D.

Working example no. 8 and working example no. 6 differ in that, while the first SiGe layer 2 has a Ge composition ratio set constant in working example no. 6, in working example no. 8 as shown in Figures 1A through 21D, Ge composition ratio x of the first SiGe layer is not constant. For example, in the first embodiment of the present working example, as shown in Figure 21A, the Ge composition ratio x of first SiGe layer 12 has an intra-layer maximum value at the interface with Si substrate 1, and the Ge composition ratio x gradually decreases.

That is to say, in the first embodiment of the present working example, the Ge composition ratio x during the first SiGe layer 12 formation step is 0.3 at the start of layer formation and thereafter gradually decreases to a final Ge composition ratio x of nearly zero. This forms a gradient composition layer that is grown to just a certain thickness (e.g., 350 nm) and is thinner than the layer thickness at which actual dislocation generation and lattice relaxation begin to become conspicuous.

For the present working example, the maximum value of intra-layer Ge composition ratio x of first SiGe layer 12 is at the interface with Si substrate 1. Thus strain energy during layer growth becomes concentrated at the interface with Si substrate 1, and when lattice relaxation occurs at the start of layer growth of second SiGe layer 3, it is possible to cause generation of many more dislocations at the interface with Si substrate 1 than at the interface with second SiGe layer 3. In this manner, dislocations can be concentrated at a position displaced from the second SiGe layer 3 surface side, and it becomes possible to lower threading dislocations and surface roughness in the same manner as during working example 6.

Moreover, in a second embodiment of the present working example as shown in Figure 21B, the Ge composition ratio x during the first SiGe layer 22 formation step is 0.2 at the start of layer formation and thereafter gradually decreases to a value of nearly zero after a certain thickness of layer growth (e.g., 175 nm), followed thereafter by a gradual increase in Ge composition ratio x to reach a final value of 0.2 at a certain thickness (e.g., 175 nm) of layer growth, thereby producing a layer of varying composition.

The thickness of this first SiGe layer 22 is also set thinner than that at which actual dislocation generation and lattice relaxation begin to become conspicuous.

Also in the second embodiment, the maximum values of intra-layer Ge composition ratio x of first SiGe layer 22 are at the interface with Si substrate 1 and at the interface with second SiGe layer 3. Thus in the same manner as for working example no. 6, it is possible to cause generation of many dislocations at the interfaces with Si substrate 1 and second SiGe layer 3.

Moreover, a third embodiment of the present working example, as shown in Figure 21C, has a Ge composition ratio x of first SiGe layer 32 that gradually increases from a value of nearly zero to a final value of 0.2 at a certain thickness (e.g., 175 nm) that is thinner than the layer thickness at which actual dislocation generation and lattice relaxation begin to become conspicuous.

Moreover, a fourth embodiment of the present working example, as shown in Figure 21D, has a Ge composition ratio x of first SiGe layer 42 that gradually increases from a value of nearly zero to a value of 0.2 at a certain thickness (e.g., 175 nm) of layer growth. Thenthe Ge composition ratio x of first SiGe layer 42 gradually decreases from 0.2 to a value of nearly zero at a certain thickness (e.g., 175 nm) of layer growth. Furthermore, thickness of first SiGe layer 42 is set thinner than the layer thickness at which actual dislocation generation and lattice relaxation begin to become conspicuous.

The below mentioned effects are obtained by the present invention.

According to the semiconductor substrate and semiconductor substrate production method of the present invention, layer thickness of the first SiGe layer is set to be thinner than twice the critical layer thickness at which dislocation generation and lattice relaxation arise due to increasing layer thickness, Ge composition ratio of the second SiGe layer is less than the maximum value of at least the Ge composition ratio of the Si layer or the Ge composition ratio of the first SiGe layer at the interface with the Si layer; and at least a portion of the second SiGe layer has a gradient composition region such that the Ge composition ratio gradually increases toward the surface. Thus dislocations can be efficiently concentrated in the vicinity of the interface between the Si substrate and the first SiGe layer and the interface between the first SiGe layer and the second SiGe layer. It then becomes possible to reduce penetrating dislocation density and surface roughness of the second SiGe layer surface.

Moreover, according to the semiconductor substrate provided with a strained Si layer and production method thereof of the present invention, due to epitaxial growth of the strained Si layer directly (or with an intervening SiGe layer) on the above mentioned SiGe layer, it becomes possible to grow the Si layer on a SiGe layer that has a good surface condition. There are few defects, and it becomes possible to form a good quality strained Si layer that has low surface roughness.

Moreover, according to the field effect transistor and field effect transistor production method of the present invention, due to formation of the channel region in the strained Si layer of the above mentioned semiconductor substrate and of the above mentioned semiconductor substrate production method of the present invention, a high performance MOSFET can be obtained with high yield due to the good quality strained Si layer.

According to the semiconductor substrate and semiconductor substrate production method of the present invention, layer thickness of the first SiGe layer is set to be thinner than twice the critical layer thickness at which dislocation generation and lattice relaxation arise due to increasing layer thickness, and the second SiGe layer has a multi-layer stacked structure consisting of alternating SiGe gradient composition layers for which the Ge composition ratio gradually increases in the direction of the surface and a SiGe constant composition layer disposed on the SiGe gradient composition layer and having the same Ge composition ratio as that of the top of the gradient composition layer, wherein the Ge composition ratio of the bottom interface of the second SiGe layer is lower than the maximum intra-layer value of the Ge composition ratio of the first SiGe layer. Therefore dislocations are concentrated efficiently in the vicinity of the interface between the Si substrate and the first SiGe layer and at the interface between the first SiGe layer and the second SiGe layer. Furthermore, dislocations can be made to run in the lateral direction without penetrating through the surface. Therefore these synergistic

effects make it possible to obtain a good quality crystalline substrate that has low penetrating defects and surface roughness.

Moreover, according to the field effect transistor and field effect transistor production method of the present invention, due to formation of the channel region in the strained Si layer of the above mentioned semiconductor substrate and of the above mentioned semiconductor substrate production method of the present invention, a high performance MOSFET can be obtained with high yield due to the good quality strained Si layer.

Claims

1. A semiconductor substrate comprising a Si substrate, a first SiGe layer on the Si substrate, and a second SiGe layer disposed on the first SiGe layer or with an optional Si layer therebetween;

wherein thickness of the first SiGe layer is smaller than twice the critical thickness causing lattice relaxation due to dislocations caused by increase of layer thickness; wherein

Ge composition ratio of the second SiGe layer is less than the maximum value of the Ge composition ratio of at least the first SiGe layer or the first SiGe layer at the interface with the Si layer; and

at least a portion of the second SiGe layer has a gradient composition region such that the Ge composition ratio gradually increases toward the surface.

2. A semiconductor substrate according to claim 1,

wherein Ge composition ratio x of the first SiGe layer is constant, and

thickness of the first SiGe layer is less than twice a critical layer thickness t_c that satisfies the following equations:

t_c (nm) = $(1.9 \times 10^{-3}/\varepsilon\ (x)^2) \cdot \ln(t_c/0.4)$,

$\varepsilon\ (x) = (a_0 + 0.200326x + 0.026174x^2)/a_0$), and

a_0 = 0.543 nm (a_0 is the Si lattice constant).

3. A semiconductor substrate according to claim 1 or claim 2,

wherein Ge composition ratio x of the first SiGe layer is greater than or equal to 0.05 and is less than or equal to 0.3.

4. A semiconductor substrate according to any one of claims 1 through 3,

wherein the second SiGe layer is disposed directly on the first SiGe layer, and

the entire second SiGe layer is a gradient composition layer having a Ge composition ratio that increases gradually in the direction of the surface.

5. A semiconductor substrate according to any one of claims 1 through 4,
wherein a strained Si layer is disposed directly on the second SiGe layer or with another SiGe layer therebetween.

6. A field effect transistor having a channel region in a strained Si layer on a SiGe layer,
wherein the field effect transistor has the channel region in the strained Si layer of the semiconductor substrate according to claim 5.

7. A method for production of a semiconductor substrate by epitaxial growth of a SiGe layer on a silicon substrate comprising the steps of:
performing a first layer forming step of epitaxial growth of a first SiGe layer on the Si substrate, and
performing a second layer forming step of epitaxial growth of a second SiGe layer directly on the first SiGe layer or with an optional epitaxial Si layer therebetween,
wherein during the first layer forming step thickness of the first SiGe layer is set to be smaller than twice the critical thickness causing lattice relaxation due to dislocations caused by increase of layer thickness,
the second SiGe layer is formed during the second layer forming step such that Ge composition ratio of the second SiGe layer is less than the maximum value of the Ge composition ratio of at least the first SiGe layer or the first SiGe layer at the interface with the Si layer, and the second SiGe layer is formed during the second layer forming step so that at least a portion of the second SiGe layer has a gradient composition region such that the Ge composition ratio gradually increases toward the surface.

8. A method for production of a semiconductor substrate according to claim 7, wherein
Ge composition ratio x of the first SiGe layer during the first formation step is constant, and
thickness of the first SiGe layer is less than twice a critical layer thickness t_c that satisfies the following equations:
t_c (nm) = $(1.9 \times 10^{-3}/\varepsilon\ (x)^2) \cdot \ln(t_c/0.4)$,

$\varepsilon(x) = (a_0 + 0.200326x + 0.026174x^2)/a_0)$, and
$a_0 = 0.543$ nm (a_0 is the Si lattice constant).

9. A method for production of a semiconductor substrate according to claim 7 or claim 8, wherein Ge composition ratio x of the first SiGe layer is greater than or equal to 0.05 and is less than or equal to 0.3.

10. A method for production of a semiconductor substrate according to any one of claims 7 through 9,

wherein the second SiGe layer is disposed directly on the first SiGe layer, and

the entire second SiGe layer is a gradient composition layer having a Ge composition ratio that increases gradually in the direction of the surface.

11. A method for production of a semiconductor substrate having a strained Si layer formed on a Si substrate with a SiGe layer therebetween, wherein the strained Si layer is formed by epitaxial growth directly on the second SiGe layer or with another SiGe layer therebetween on the semiconductor substrate produced according to any one of claims 7 through 10.

12. A method for production of a field effect transistor having a channel region in a strained Si layer formed by epitaxial growth on a SiGe layer, wherein the channel region is formed in the strained Si layer of the semiconductor substrate formed according to the method of claim 11.

13. A semiconductor substrate having a SiGe layer formed on a Si substrate, wherein the semiconductor substrate is formed by the production method according to any one of claims 7 through 10.

14. A semiconductor substrate having a strained Si layer formed on a Si substrate with a SiGe layer therebetween, wherein the semiconductor substrate is formed by the production method according to claim 11.

15. A field effect transistor having a channel region in a strained Si layer formed by epitaxial growth on a Si substrate, wherein the field effect transistor is produced by the field effect transistor production method according to claim 12..

16. A semiconductor substrate comprising a Si substrate, a first SiGe layer on the Si substrate, and a second SiGe layer disposed on the first SiGe layer or with an optional Si layer therebetween,

wherein thickness of the first SiGe layer is smaller than twice the critical thickness causing lattice relaxation due to dislocations caused by increase of layer thickness;

the second layer SiGe layer has a multi-layered structure formed by alternately and contiguously stacking of a SiGe gradient layer having a Ge composition ratio that increases gradually toward the surface and thereupon a SiGe layer of constant composition having the same Ge composition ratio as the upper interface of the gradient composition layer, and

the Ge composition ratio of the bottom interface of the second SiGe layer is less than the maximum value of the Ge composition ratio within the first SiGe layer.

17. A semiconductor substrate according to claim 16, wherein the Ge composition ratio x of the first SiGe layer is constant, and thickness of the first SiGe layer is less than twice a critical layer thickness t_c that satisfies the following equations:

$$t_c\,(\mathrm{nm}) = (1.9 \times 10^{-3}/\varepsilon\,(x)^2) \cdot \ln(t_c/0.4),$$

$\varepsilon(x) = (a_0 + 0.200326x + 0.026174x^2)/a_0)$, and
$a_0 = 0.543$ nm (a_0 is the Si lattice constant).

18. A semiconductor substrate according to claim 16 or claim 17, wherein the Ge composition ratio x of the first SiGe layer is greater than or equal to 0.05 and is less than or equal to 0.3.

19. A semiconductor substrate according to any one of claims 16 through 18, wherein a strained Si layer is disposed directly on the second SiGe layer or another SiGe layer is disposed therebetween.

20. A field effect transistor having a channel region in a strained Si layer disposed on a SiGe layer, wherein the channel region is in the strained Si layer of the semiconductor substrate according to claim 19.

21. A method for production of a semiconductor substrate by epitaxial growth of a SiGe layer on a silicon substrate comprising the steps of:

performing a first layer forming step of epitaxial growth of a first SiGe layer on the Si substrate, and

performing a second layer forming step of epitaxial growth of a second SiGe layer directly on the first SiGe layer or with an optional epitaxial Si layer therebetween,

wherein during the first layer forming step thickness of the first SiGe layer is set to be smaller than twice the critical thickness causing lattice relaxation due to dislocations caused by increase of layer thickness,

the second SiGe layer forming step, to form the second SiGe layer such that Ge composition ratio has a gradient in the layer growth direction and changes step-wise, consists of repeating the following alternating steps a multiple number of times with a continuous Ge composition ratio: a step of epitaxial growth of a gradient composition layer of SiGe such that the Ge composition ratio increases gradually toward the surface, and a step of epitaxial growth of the constant composition layer of SiGe on the gradient composition layer at the final Ge composition ratio of the gradient composition layer, and

Ge composition ratio of the bottom interface of the second SiGe layer is lower than the maximum value of the Ge composition ratio in the first SiGe layer.

22. A method for production of a semiconductor substrate according to claim 21, wherein the Ge composition ratio x of the first SiGe layer is constant, and thickness of the first SiGe layer is less than twice a critical layer thickness t_c that satisfies the following equations:

t_c (nm) = $(1.9 \times 10^{-3}/\varepsilon\ (x)^2) \cdot \ln(t_c/0.4)$,

$\varepsilon\ (x) = (a_0 + 0.200326x + 0.026174x^2)/a_0$), and

a_0 = 0.543 nm (a_0 is the Si lattice constant).

23. The semiconductor production method according to claim 21 or 22, wherein Ge composition ratio x of the first SiGe layer is greater than or equal to 0.05 and is less than or equal to 0.3.

24. A method for production of a semiconductor substrate by forming a strained Si layer on a Si substrate and a SiGe layer therebetween, wherein the strained Si layer is formed by epitaxial growth directly on the second SiGe layer, or with another SiGe layer therebetween, of the semiconductor substrate produced by the semiconductor production method according to any one of claims 21 through 23.

25. A method for production of a field effect transistor by forming a channel region in a strained Si layer formed by epitaxial growth on a SiGe layer, wherein the channel region is formed in the strained Si layer of the semiconductor substrate produced by the semiconductor substrate production method according to claim 24.

26. A semiconductor substrate having a SiGe layer formed on a Si substrate, wherein the semiconductor substrate is produced by the semiconductor substrate production method according to any one of claims 21 through 23.

27. A semiconductor substrate having a strained Si layer formed on a Si substrate and a SiGe layer therebetween, wherein the semiconductor substrate is produced by the semiconductor substrate production method according to claim 24.

28. A field effect transistor having a channel region formed in a strained Si layer formed by epitaxial growth on a SiGe layer, wherein the semiconductor substrate is produced by the semiconductor substrate production method according to claim 25.

Figure 1
[*Insert drawing.*]

Figure 2
[*Insert graph. The vertical axis label is "Ge composition ratio", and the horizontal axis label is "Thickness".*]

Figure 3
[*Insert drawing.*]

Figure 4
[*Insert graph. The vertical axis label is "Ge composition ratio", and the horizontal axis label is "Thickness".*]

Figure 5

[*Insert graph. The vertical axis label is "Ge composition ratio", and the horizontal axis label is "Thickness".*]

Figure 6

[*Insert graph. The vertical axis label is "Ge composition ratio", and the horizontal axis label is "Thickness".*]

Figure 7

[*Insert graph. The vertical axis label is "Ge composition ratio", and the horizontal axis label is "Thickness".*]

Figure 8

[*Insert graph. The vertical axis label is "Composition (Si(1-x)Gex)", the horizontal axis label is "Depth (microns)", the top peak label is "Average 30.6% Ge", and the bottom peak label is "Average 14.3% Ge".*]

Figure 9

[*Insert graph. The vertical axis label is "Penetrating dislocation density (etch pit density) [$\times 10^5$ pits/cm^2]", the horizontal axis label is "Thickness of first SiGe layer [nm]", the top curve label is "Ge composition ratio = 0.2", the middle curve label is "Ge composition ratio = 0.15", and the bottom curve label is "Ge composition ratio = 0.1".*]

Figure 10

[*Insert graph. The vertical axis label is "Surface roughness [nm]", the horizontal axis label is "Thickness of first SiGe layer [nm]", the top curve label is "Ge composition ratio = 0.2", the middle curve label is "Ge composition ratio = 0.15", and the bottom curve label is "Ge composition ratio = 0.1".*]

Figure 11

[*Insert image.*]

Replacement sheet (Rule 26)

Figure 12

[*Insert image.*]

Replacement sheet (Rule 26)

Figure 13

Layer thickness 350 nm	Ge composition ratio 0.2 RMS (nm)
conventional technology	2.73
working example no. 2	1.69
working example no. 3	1.62
working example no. 4	1.89
working example no. 5	2.09

Figure 14

[*Insert graph. The vertical axis label is "Penetrating dislocation density (etch pit density) [$\times 10^5$ pits/cm^2], the horizontal axis label is "Thickness of first SiGe layer [nm]".*]

Figure 15

[*Insert graph. The vertical axis label is "Surface roughness [nm], the horizontal axis label is "Thickness of first SiGe layer [nm]".*]

Figure 16
[*Insert graph. The vertical axis label is "Ge composition ratio", and the horizontal axis label is "Thickness".*]

Figure 17
[*Insert drawing.*]

Figure 18

[*Insert graph. The vertical axis label is "Ge composition ratio", and the horizontal axis label is "Thickness".*]

Figure 19

[*Insert graph. The vertical axis label is "Ge composition ratio", and the horizontal axis label is "Thickness".*]

Figure 20

Figure 21A

[*Insert graph. The vertical axis label is "Ge composition ratio", and the horizontal axis label is "Thickness".*]

Figure 21B

[*Insert graph. The vertical axis label is "Ge composition ratio", and the horizontal axis label is "Thickness".*]

Figure 21D

[*Insert graph. The vertical axis label is "Ge composition ratio", and the horizontal axis label is "Thickness".*]

Figure 21D

[*Insert graph. The vertical axis label is "Ge composition ratio", and the horizontal axis label is "Thickness".*]

Figure 22

[*Insert graph. The vertical axis label is "Penetrating dislocation density [dislocations/cm^2]", the horizontal axis label is "Thickness of first SiGe layer (nm)", and the labels within the chart say "STD (conventional technology)", "Comparative example", and "Working example no. 1".*]

Figure 23

[*Insert graph. The vertical axis label is "Surface roughness [nm]", the horizontal axis label is "Thickness of first SiGe layer (nm)", and the labels within the chart say "STD (conventional technology)", "Comparative example", and "Working example no. 1".*]